LISTING OF THE CLAIMS

This listing of claims, amended as indicated below, will replace all prior versions, and listings, of claims in the application

1. **(Canceled)**

2. **(Currently Amended)** An endoscope apparatus according to claim ~~1~~ 14, wherein said first processor is a digital signal processor constructed as an integrated circuit.

3. **(Currently Amended)** An endoscope apparatus according to claim ~~1~~ 14, wherein said delay circuit is variable in its delay time.

4. **(Original)** An endoscope apparatus according to claim 3, wherein said delay circuit comprises a multistage buffer circuit connected in series and a circuit for selecting the number of stages of said multistage buffer circuit.

5. **(Original)** An endoscope apparatus according to claim 3, comprising a second processor for setting the delay time of said delay circuit.

6. **(Original)** An endoscope apparatus according to claim 5, comprising:
a switch for specifying said delay time; and
said second processor setting said delay time depending on the condition of said switch.

7. **(Original)** An endoscope apparatus according to claim 5, comprising:
a switch for setting information from which said delay time can be derived; and
said second processor setting said delay time depending on the condition of said switch.

8. **(Original)** An endoscope apparatus according to claim 7:

wherein information from which said delay time can be derived includes information indicating length of an insert portion of said endoscope.

9. **(Previously Presented)** An endoscope apparatus according to claim 7: wherein information from which said delay time can be derived includes identification information for identifying a type of said endoscope.

10. **(Currently Amended)** An endoscope apparatus according to claim 5, ~~comprising:~~ wherein:

said endoscope ~~including~~ includes an information acknowledgment portion for giving information indicating said delay time to said second processor; and

said second processor ~~setting~~ is operative to set said delay time ~~depending~~ based on information ~~acknowledged from~~ provided by said information acknowledgment portion.

11. **(Currently Amended)** An endoscope apparatus according to claim 5, ~~comprising:~~ wherein:

said endoscope ~~including a~~ includes an information acknowledgment portion for giving information from which said delay time can be derived to said second processor; and

said second processor is operative to set said delay time ~~depending~~ based on information ~~acknowledged from~~ provided by said information acknowledgment portion.

12. **(Currently Amended)** An endoscope apparatus according to claim 11:

wherein information from which said delay time can be derived includes information indicating a length of ~~an insert~~ the insertion portion of said endoscope.

13. **(Original)** An endoscope apparatus according to claim 11:

wherein information from which said delay time can be derived includes identification information for identifying a type of said endoscope.

14. (New) An endoscope apparatus, comprising:

an endoscope portion including a part that is insertable into a body or object having internal parts that require imaging; and

a separate video processor removably connected to the endoscope portion by a signaling cable, the video processor including therein:

a synchronizing signal generator;

a first drive signal generator responsive to the synchronizing signal to generate a first drive signal for an imaging device located in said endoscope portion, and to transmit said first drive signal to said endoscope portion through said signaling cable;

a video signal extracting portion for obtaining a first video signal from an imaging signal obtained in said imaging device and transmitted from said endoscope portion through said signaling cable;

a second drive signal generator portion responsive to the synchronizing signal to generate a second drive signal for controlling a timing when said video signal extracting portion obtains said first video signal from said imaging signal;

a first processor, the first processor including at least a part of a circuit for obtaining, from said first video signal, a second video signal that can be displayed on a monitor; and

an adjustable delay circuit including a first portion coupled between said synchronization signal generator and said first drive signal generator and a second portion coupled between said synchronization signal generator and said second drive signal generator,

said adjustable delay circuit being operable to provide selectable delays for synchronization signals provided to said first and second drive signal generators.